Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

.011 x .011”

**.017**

**.017”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .011” X .011”**

**Backside Potential: CATHODE**

**Mask Ref: TRR**

**APPROVED BY: DK DIE SIZE .017” X .017” DATE: 10/21/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .007” P/N: 1N3595**

**DG 10.1.2**

#### Rev B, 7/1